UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,690	08/19/2003	Yoshiyuki Kurokawa	0553-0323.01	5081

7590 02/09/2005

Edward D. Manzo
Cook, Alex, McFarron, Manzo,
Cummings & Mehler, Ltd.
200 West Adams St., Ste. 2850
Chicago, IL 60606

EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,690	KUROKAWA ET AL.	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,10-13,16-19,21,24-27 and 43-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,10-13,16-19,21,24-27 and 43-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/156,512.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on December 27, 2004 in which claims 1 and 43 were amended, has been entered of record.

2. The indicated allowability of claims 1, 4-7, 10-13, 16-19, 21, 24-27 and 43-50 is withdrawn in view of the newly discovered reference(s) to Tzeng, Uenoyama, Kachelmeier and Acovic. Rejections based on the newly cited references follow.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. However, the following grammatical errors were found which suggest a thorough review of the specification is needed:

Page 1, line 7, "the invention is also relates"

Page 1, line 20, "future development in future is expected."

Page 2, line 14, "which leads increase of a writing time"

Page 2, line 19, "manufacturing processes is improved".

Page 23, lines 17-18, "NOR type of flush memory."

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 7 and 43 are objected to because of the following informalities: claim 7 includes limitations which repeat themselves – line 4 states "a first region and a second region formed in the channel forming region;" and line 9 repeats the limitation. Claim 43, line 13 should be amended to have --in-- inserted after "not". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5, dependent from claim 1, cites specific limitations for the structure of the substrate. However, because of claim 1's amendments, it is not clear how the thin film transistor of claim 1 which is formed on an insulating surface, can be further limited such that the substrate is single crystal. Alternatively, claim 5 is objected to as the limitations therein fail to further limit that of claim 1. The same analysis is applied to claim 45, dependent from 42.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 7 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,215,934 to Tzeng. Tzeng teaches, with reference to figures 5 and 6, a memory transistor comprising:

an active layer 20, comprising a source 36, drain 37 and channel forming region (inherently formed between 36 and 37);

a first region 25a and a second region 25b formed in the channel forming region;

a first insulating film 30/31 formed on the active layer;

a floating gate 33 formed on the first insulating film;

a second insulating film (not shown, col. 6, lines 23-28); and

a control gate 35 formed on the second insulating film;

wherein a concentration of impurity elements in the first region is larger than a concentration of impurity elements in the second region (see the limitations of Tzeng, claim 26, citing that the threshold voltages differ between channel portions, and see col. 7, lines 2-6 teaching that the threshold difference is achieved by ion implantation).

Regarding claim 10, this claim cites functional limitations which may be achieved by the structure of Tzeng; as taught by applicant, the function of storing multi-value information is achieved by applying different programming voltages, not by a difference in structure over that

taught by Tzeng. Regarding claim 11, Tzeng teaches that the substrate 20 is single crystal silicon (col. 5, lines 39-41). Regarding claim 12, this claim merely cites intended uses of the structure anticipated by Tzeng and does not distinguish over Tzeng.

7. Claims 13, 16-19, 21, 24-27 and 47-50 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,973,357 to Uenoyama et al. Uenoyama teaches, with reference to figures 1 and 2, a memory cell comprising:

an active layer comprising a first channel forming region ER1 interposed between a source region 31 and a source/drain region 34, and a second channel forming region 35 interposed between the source/drain region 34 and a drain region 30;

a first insulation film 5 formed on the active layer;

a first floating gate 1 (above region 20) and a second floating gate 1 (above ER1) formed on the first insulating film 5;

a second insulating film 4 formed on the first floating gate and the second floating gate; and

a first control gate 3 and a second control gate (also 3) formed on the second insulating film,

wherein a thickness of the first insulating film on the second channel forming region 35 is thinner than a thickness of the first insulating film on the first channel forming region ER1;

wherein the first and second floating gates and the first and second control gates are respectively connected to each other (as seen in Fig. 1, the control and floating gates are continuous).

Regarding claims 21 and 47, Uenoyama may be interpreted to teach that the region 35 is the first channel forming region and ER1 is the second channel forming region such that the first channel forming region has a larger concentration of impurity elements than does the second region and thus the threshold voltage of the second region is higher than that of the first region.

Regarding claims 16, 24 and 48, these claims cite functional limitations which may be achieved by the structure of Uenoyama; as taught by applicant, the function of storing multi-value information is achieved by applying different programming voltages, not by a difference in structure over that taught by Uenoyama. Regarding claims 17, 25 and 49, it is considered inherent that the device of Uenoyama is formed on a single crystal silicon substrate. Regarding claims 18, 26 and 50, these claims merely cite intended uses of the structure anticipated by Uenoyama and do not distinguish over Uenoyama. Regarding claim 19, the threshold voltage of the first and second channel forming regions ER1 and 35 are different.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4-6, 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,897,354 to Kachelmeier in view of 5,411,905 to Acovic et al. Kachelmeier teaches in figure 1 a memory device comprising:

an active layer 1 comprising a source region 2, a drain region 3 and a channel forming region (inherently formed between the source and drain);

a first insulating film 10 formed on the active layer;

a floating gate 9 formed on the first insulating film;

a second insulating film 7 formed on the floating gate;

a control gate 6 formed on the second insulating film and not in contact with the first insulating film; and

a first region and a second region included in the channel forming region, wherein a thickness of the first insulating film 10 on the second region (the region closer to the source 2) is thinner than a thickness of the first insulating film 10 on the first region (the region closer to the drain 3) and thus the threshold voltage of the second region is larger than a threshold voltage of the first region (an inherent property, dependent on the thickness of the gate oxide).

However, Kachelmeier does not teach that the device's active layer is formed on an insulating layer to thus form a thin film transistor. Acovic teaches in figure 5 that it is well known in the art to form an EEPROM (memory) device on an SOI substrate (active layer 12 formed oxide layer 10). Kachelmeier and Acovic are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Kachelmeier using an SOI substrate. The motivation for doing so is that an SOI substrate prevents substrate current and thus no interference between memory cells (col. 2, lines 64-68). Therefore, it would have been obvious to combine Kachelmeier and Acovic to obtain the invention of claims 1, 4-6 and 43-46.

Regarding claims 4 and 44, this claim cites functional limitations which may be achieved by the structure of Kachelmeier; as taught by applicant, the function of storing multi-value information is achieved by applying different programming voltages, not by a difference in structure over that taught by Kachelmeier. Regarding claims 5 and 45, as best understood, Acovic makes obvious forming the device on an SOI substrate. Regarding claims 6 and 46, these claims merely cite intended uses of the structure made obvious by Kachelmeier and Acovic and do not distinguish over them.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 7, 10-13, 16-19, 21, 24-27, and 47-50 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,621,130. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the instant application are broader in scope than those of the issued patent (e.g. patented independent claim 1 cites both a concentration and thickness difference between the first and second regions of the channel, whereas the instant

claims cite either a thickness or concentration difference). For this reason, the instant claims are considered "anticipated" by the patented reference.

11. Claims 1, 4-6 and 43-46 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,621,130 in view of 5,411,905 to Acovic. The claims of the issued patent teach in more narrow terms the limitations of the instant claims but do not teach that the device is formed as a TFT/on an SOI substrate. Acovic teaches such an SOI substrate and motivates its use in that it eliminates substrate current and thus cross-talk. As such, it would have been obvious to modify the claims of patent '130 with the teaching of Acovic to obtain the invention of the subject claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited art teach structures similar to that instantly claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax number is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER